

PATENT ABSTRACTS OF JAPAN

(11) Publication number: 07046089 A

(43) Date of publication of application: 14.02.95

(51) Int. Cl. H03K 3/286

(21) Application number: 05184870

(22) Date of filing: 27.07.93

(71) Applicant: SANYO ELECTRIC CO LTD

(72) Inventor: MURAYAMA MAKOTO

(54) T-TYPE FLIP-FLOP CIRCUIT

(57) Abstract:

**PURPOSE:** To easily prevent abnormal oscillation by making an unbalanced current flow to an interruption means constituted of third and sixth amplifiers and interrupting an oscillation loop constituted of first, second, forth and fifth differential amplifiers.

**CONSTITUTION:** The third and sixth differential amplifiers 11 and 17 at the time of non-signal are turned to an unbalanced state and a current in transistors 22 and 29 and the current in the transistors 23 and 30 are differentiated. The change is performed approximately to an amount by which the differential amplifiers constituting the oscillation loop can not inverse-output signals at a level required for oscillation. At the time, the third and sixth differential amplifiers 11 and 17 can interrupt the oscillation loop in the case of the unbalance of either polarity. At the time even when DC balance is changed, a normal operation is not affected. That is, the level of clock signals impressed to input terminals 1 and 2 is sufficiently raised and the differential amplifiers 11 and 17 are switching operated exceeding the level even when offset is present. Thus, the T-FF capable of preventing the oscillation at the time of non-signal and

immediately moving to the normal operation can be obtained while hardly requiring additional elements.

COPYRIGHT: (C)1995,JPO

